occurrences of the word "oxide".

In Claim 42, at line 3, insert --gate-- before "oxide".

Please cancel Claim 43.

At Claim 53, at line 1, delete "said" and substitute "the"; at line 3, delete "part".

Please amend Claims 17, 30-32, 46 and 52 as follows:

17. (amended) A trench DMOS transistor cell, comprising:

a substrate of a first conductivity type, said substrate having a surface;

an epitaxial layer of said first conductivity type formed on said surface of said substrate, said epitaxial layer having a top surface and a bottom surface, said epitaxial layer having a substantially uniform initial dopant concentration at formation;

a body region of a second conductivity type formed in said epitaxial layer, said body region extending, as measured from said top surface of said epitaxial layer, to a first depth d_{max} at a first location and to a depth of d at a second location, where d is less than d_{max}, said first and second locations being separated by a predetermined horizontal distance;

a source region of said first conductivity type formed in said expitaxial layer above a portion of said body region, said portion of said body region being located between said second location and said source region; and

a trench formed in said epitaxial layer, having substantially vertical side walls, extending from said top surface of said epitaxial layer to a depth d_{tr}, said depth d_{tr} being less than said depth d_{max}, and greater than said depth d, said trench being (i) closer to said second location than said first location, and (ii) [said trench being] horizontally adjacent said source region.

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SKJERVEN, MORRILL,
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& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

30. (Amended) A trench DMOS transistor cell, comprising:

a substrate of semiconductor material of [heavily doped] a first electrical conductivity type having a top surface;

a first covering layer of semiconductor material of said first electrical conductivity type, said first covering layer (i) having a dopant concentration less than that of said substrate, (ii) having a top surface and (iii) being contiguous to and overlying the substrate top surface;

a second covering layer of semiconductor material of second electrical conductivity type having a top surface and being contiguous to the top surface of the first covering layer and extending vertically downward from the top surface of the first covering layer into an upper portion of the first covering layer;

a third covering layer of semiconductor material of [heavily doped] said first electrical conductivity type having a top surface and being contiguous to and partly overlying the top surface of the second covering layer, [where a portion of the second covering layer is heavily doped and this portion extends vertically upward through the third covering layer to the top surface thereof and forms an exposed pattern of the second covering layer in the top surface of the third covering layer, and] where the maximum depth [of the heavily doped portion] of the second covering layer relative to the top surface of the third covering layer is a depth d_1;

a trench, having side walls and a bottom wall [bottom walls and], said side walls extending vertically downward from the top surface of the third covering layer through the third and second covering layers and through a portion of, but not all of, the first covering layer, where the trench has a maximum depth relative to the top

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SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
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FAX (408) 453-7979

surface of the third covering layer equal to a second depth d_2 and d_2 is less than d_1, where the trench in horizontal cross section is approximately a polygonal stripe, and where this polygonal stripe laterally surrounds and is spaced apart from the exposed pattern of the second covering layer at the top surface of the third covering layer;

a layer of oxide positioned within the trench and contiguous to the bottom walls and side walls of the trench so that portions, but not all, of the trench are filled with the oxide layer;

electrically conducting semiconductor material, contiguous to the oxide layer and positioned within the trench so that the oxide layer lies between the electrically conducting semiconductor material and the bottom and side walls of the trench; and

three electrodes that are electrically coupled to the electrically conducting semiconductor material in the trench, to the third covering layer and to the substrate, respectively;

wherein the difference d_1-d_2 of said first and second depths d_1 and d_2 is sufficient to force junction breakdown away from the trench and into the [heavily doped portion of the second covering layer].

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~~31~~. (Amended) A trench DMOS transistor cell as in Claim [31] ~~30~~, wherein said trench comprises rounded edges of oxidized material[, where said bottom surfaces and said side surfaces of said trench meet said top surface of said third covering layer and where said side surfaces of said trench meet with one another].

32. (Amended) A trench DMOS transistor cell, comprising:

a substrate;

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an epitaxial layer above the substrate;

a trench in the epitaxial layer, the trench having substantially vertical side walls and having a predetermined depth d_{tr}; and

a body region in the epitaxial layer, the body region having a predetermined maximum depth d_{max},

wherein the depth d_{tr} is less than the depth d_{max}, and

wherein the difference between the depth d_{max} and the depth d_{tr} is sufficient to force junction breakdown away from the trench and into the epitaxial layer.

46. (Amended) A transistor, comprising:

a first region of a first conductivity type;

a second region of a second conductivity type over said first region;

a third region of said first conductivity type such that said first and third regions are separated by said second region;

a trench, having substantially vertical side walls, extending through said third and second regions; and

a gate in said trench; wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.

52. (Amended) A transistor, comprising:

a first region of a first conductivity type;

a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;

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SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
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FAX (408) 453-7979

a third region of a second conductivity type over said second region, said second and third regions forming a junction;

a fourth region of said first conductivity type over said third region;

a trench, having substantially vertical side walls, extending through said fourth and third regions; and

a gate in said trench; wherein a deepest part of said third region is laterally spaced from said trench; and wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.

Please add Claims 54-66 as follows:

54. A semiconductor device comprising:

a semiconductor body having a trench therein of depth d_{tr} and substantially vertical side walls, said semiconductor substrate including a body region, said body region having a maximum depth of d_{max}, wherein said maximum depth d_{max} being greater than said depth d_{tr} by an amount sufficiently large to force junction breakdown away from said trench.

55. A semiconductor device as in Claim 54, further comprising a substrate of a first conductivity type, an epitaxial layer of said first conductivity type and wherein said body region is of a second conductivity type.

56. A semiconductor device as in claim 55 wherein the epitaxial layer has a top surface and the body region extends from the epitaxial layer top surface into an upper portion of

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SKJERVEN, MORRILL,
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& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
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the epitaxial layer.

38 34
~~37~~. A semiconductor device as in claim ~~55~~ wherein a source region is formed in said epitaxial layer.

58. A semiconductor device as in Claim ~~54~~ wherein said body region extends upward through the epitaxial region and forming an exposed pattern at the epitaxial layer top surface.

40 39
~~59~~. A semiconductor device as in Claim ~~58~~ wherein the trench surrounds the exposed pattern of the body region.

41 35
~~60~~. A semiconductor device as in Claim ~~54~~ wherein said trench has side walls, said semiconductor device having an oxide layer on said trench walls, and wherein said oxide layer is etched to create rounded corners in said trench.

42 41
~~61~~. A semiconductor device as in Claim ~~60~~, further comprising a gate oxide layer within the trench.

43 42
~~62~~. A semiconductor device as in Claim ~~61~~ further comprising an electrically conducting material contiguous to said gate oxide layer, wherein said gate oxide layer is located between said electrically conducting material and said trench.

44 42
~~63~~. A semiconductor device as in Claim ~~61~~, further comprising:

a first polysilicon layer on a portion of said gate oxide layer;

a second oxide layer on a portion of said first polysilicon layer;

a second polysilicon layer on a portion of said second oxide layer; and

a metal layer wherein said ~~second~~ first polysilicon layer

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25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
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FAX (408) 453-7979